CG65050TBD

Description

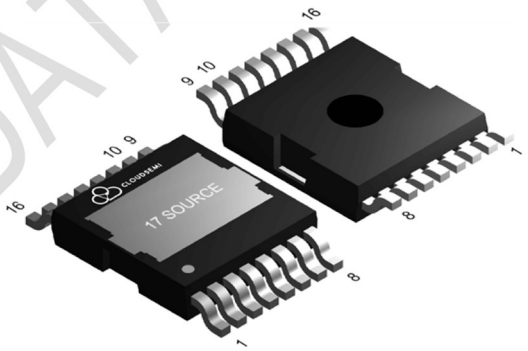
CG65050TBD is a GaN-on-Si enhancement-mode power transistor in TO-Leaded top-side cooling package (TOLT). The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The TOLT package offers superior heat dissipation, low parasitic resistance/inductance and high solderability, which can fully release device potential and make GaN better apply to industrial applications.

Applications

- AC-DC converters, DC-DC converters
- Bridgeless totem pole PFC, data center, telecom, network SMPS
- Uninterruptable power supplies (UPS)
- Solar inverters, energy storage systems
- On board charger (OBC)
- Charging pile
- Traction inverter
- Industrial motor drives

Features

- 650V GaN enhancement-mode power switch
- $R_{DS(on),\ max}$ 50mΩ
- Recommended gate drive voltage 0V ~ 6V
- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection, HBM class 2, CDM class C3
- RoHS, Pb-free, REACH-compliant



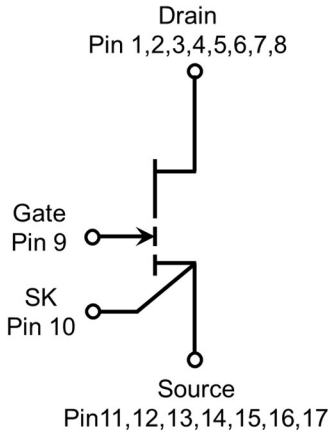


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	650	V
$R_{DS(on),\ max}$	50	mΩ
$Q_{G,\ typ}$	9.2	nC
$I_{D,\ Pulse}$	80	A
Q_{OSS} @ 400 V	82	nC
Q_{rr}	0	nC

Table 2 Ordering Information

Ordering Code	Package	Marking	Packing
CG65050TBD	TOLT	CG65050TBD	Reel

Table of Contents

1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

Table 3 Maximum ratings

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	V_{GS} = 0 V, I_D = 10 μA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	850	V	V_{GS} = 0 V, V_{DS} = 850 V
Continuous current, drain-source	I_D	-	-	40	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	80	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	35	A	T_c = 150 °C; V_G = 6 V
Gate-source voltage, continuous [3]	V_{GS}	-7	-	+7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20	-	+10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-		W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.
2. Pulse width = 10 μs.
3. The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 8.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-		°C/W	
Thermal resistance, junction-ambient	R_{thJA}	-	-		°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless otherwise specified.

Table 5 Static characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.1	1.7	2.6	V	V_{DS} = V_{GS}, I_D = 10 mA; T_j = 25 °C
		-	1.9	-		V_{DS} = V_{GS}, I_D = 10 mA; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	3	80	μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	120	-		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	240	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	39	50	mΩ	V_{GS} = 6 V; I_D = 20 A; T_j = 25 °C
		-	86	-	mΩ	V_{GS} = 6 V; I_D = 20 A; T_j = 150 °C
Gate resistance	R_G	-	1.1	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	312	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Output capacitance	C_{oss}	-	82	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Reverse transfer capacitance	C_{rss}	-	0.9	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	140	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	206	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	82	-	nC	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Output Capacitance Stored Energy	E_{OSS}	-	11	-	μJ	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	9.2	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 40 A
Gate-source charge	Q_{GS}	-	2.4	-	nC	
Gate-drain charge	Q_{GD}	-	2.4	-	nC	
Gate plateau voltage	V_{plat}	-	2.8	-	V	V_{DS} = 400 V; I_D = 40 A

Table 8 Reverse conduction characteristics

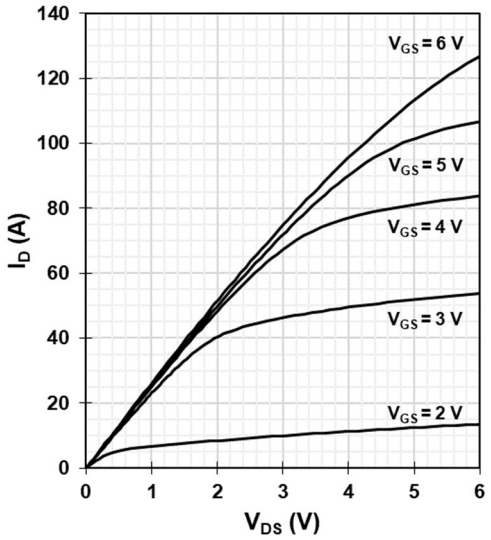
Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	3.9	-	V	V_{GS} = 0 V; I_{SD} = 40 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	60	-	A	V_{GS} = 6 V
Reverse recovery charge [1]	Q_{rr}	-	0	-	nC	I_{SD} = 40 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{OSS}

4 Electrical characteristics diagrams

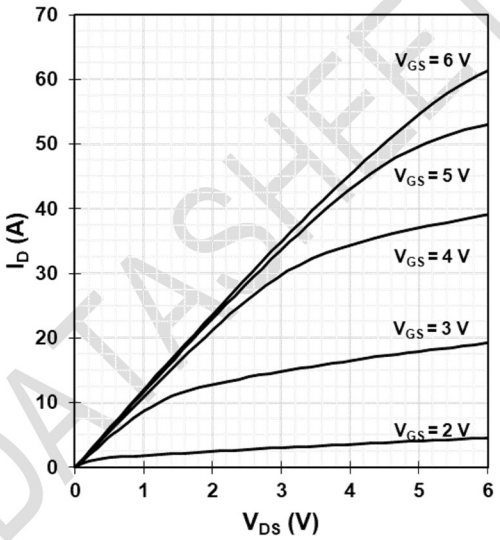
at T_j = 25 ºC, unless otherwise specified.

Figure 1 Typ. output characteristics



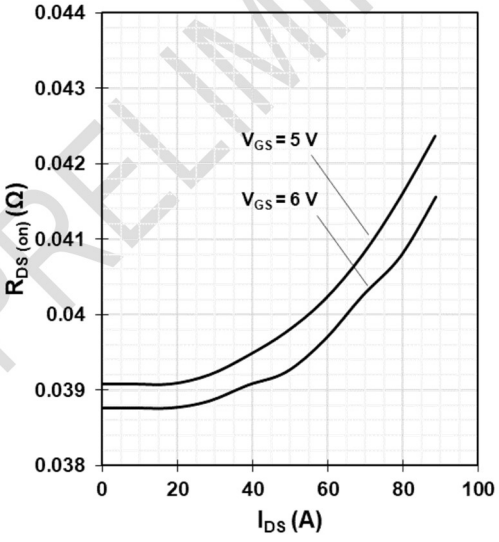
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 ºC

Figure 2 Typ. output characteristics



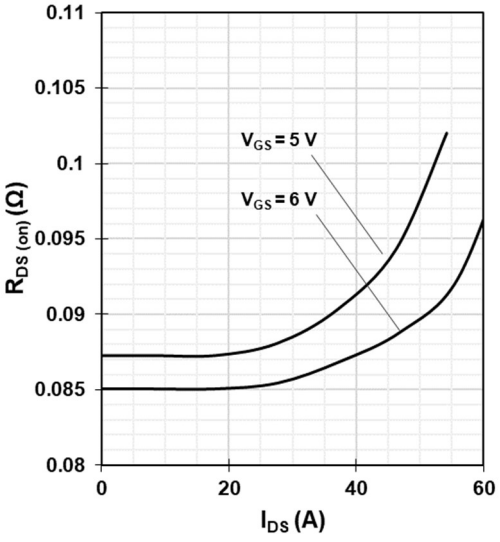
$I_D = f(V_{DS}, V_{GS})$; T_j = 150 ºC

Figure 3 Typ. drain-source on-state resistance



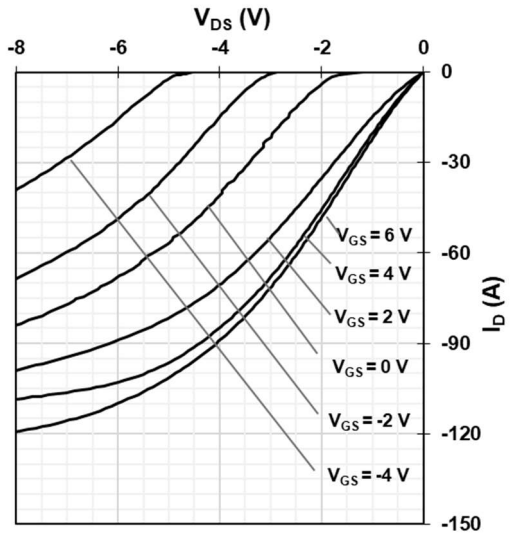
$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 25 ºC

Figure 4 Typ. drain-source on-state resistance



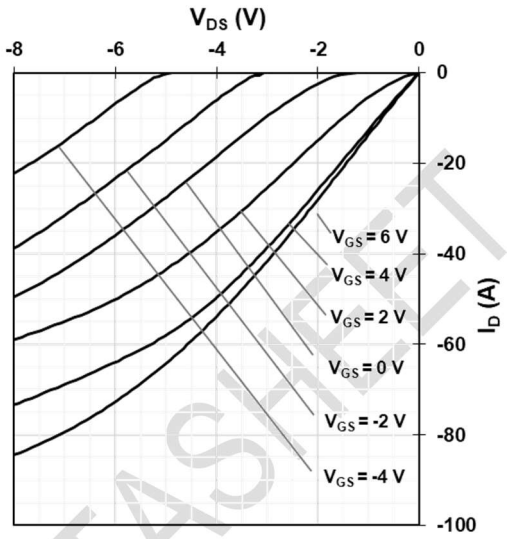
$R_{DS(on)} = f(I_{DS}, V_{GS})$; T_j = 150 ºC

Figure 5 Typ. channel reverse characteristics



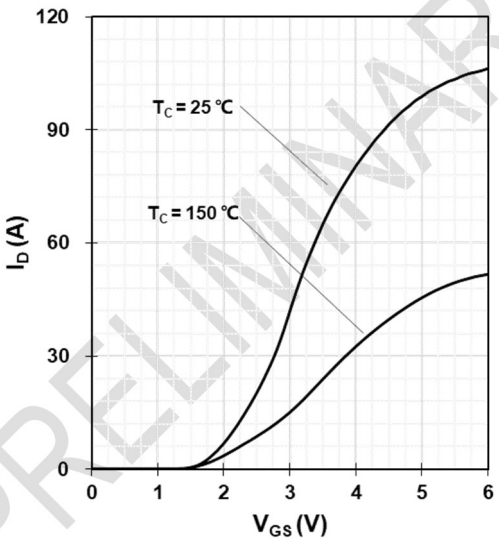
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 6 Typ. channel reverse characteristics



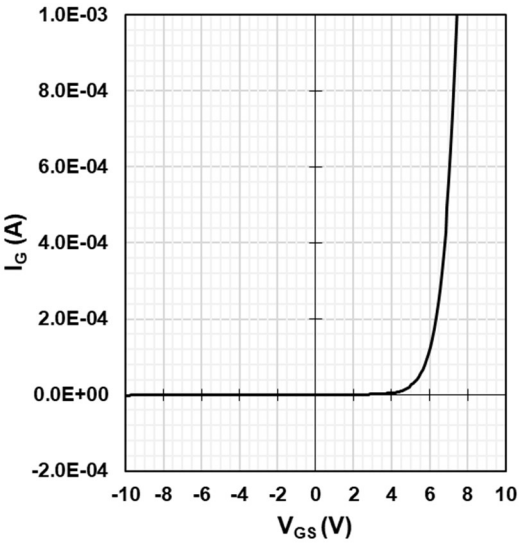
$I_D = f(V_{DS}, V_{GS})$; T_j = 150 °C

Figure 7 Typ. transfer characteristics



$I_D = f(V_{GS})$; V_{DS} = 5 V

Figure 8 Typ. gate-to-source leakage



$I_G = f(V_{GS})$; V_D = open

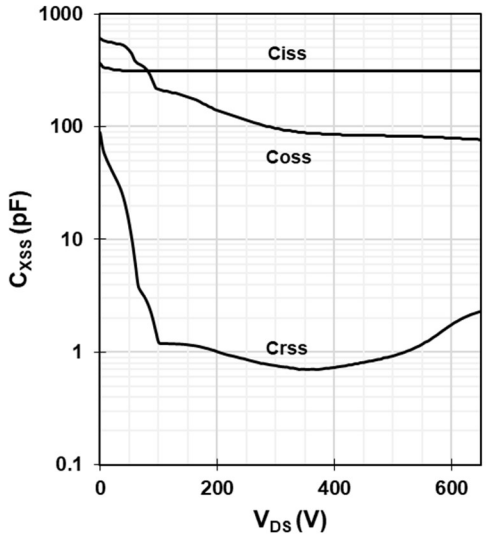
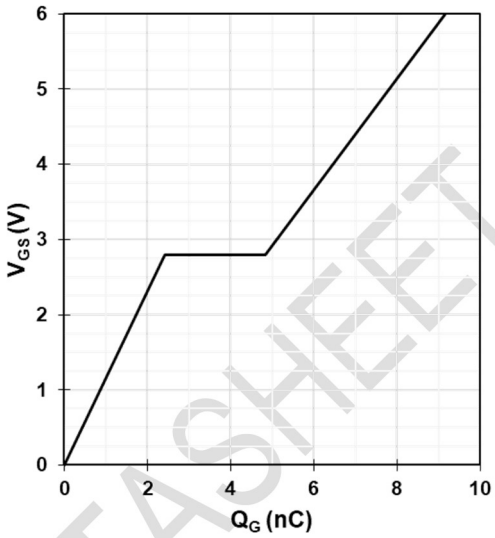
Figure 9 Typ. capacitances	Figure 10 Typ. gate charge
	
C_{XSS} = f(V_{DS}); Freq. = 1 MHz	V_{GS} = f(Q_G); V_{DS} = 400 V; I_D = 40 A

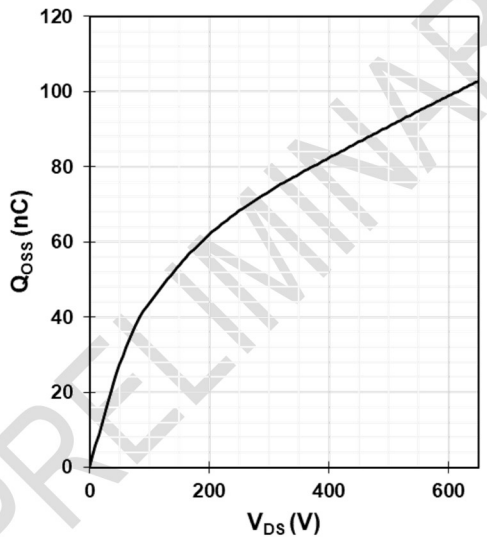
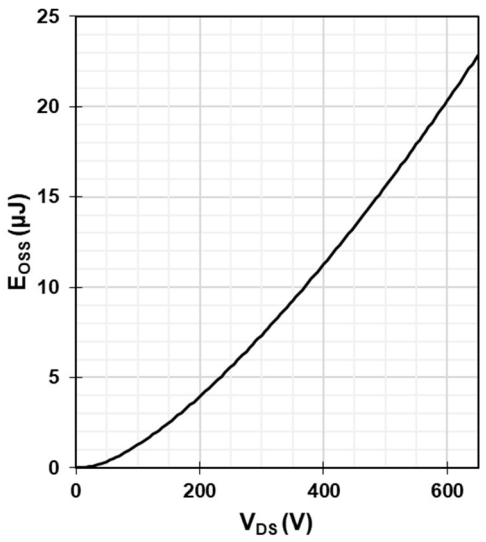
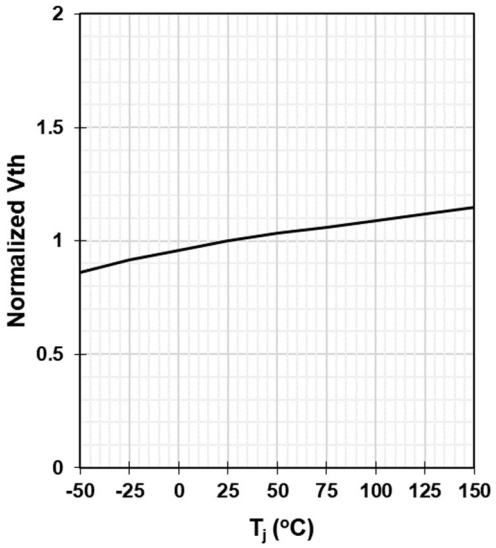
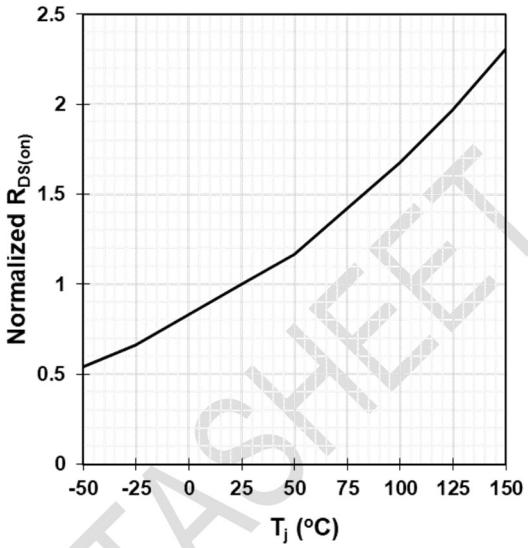
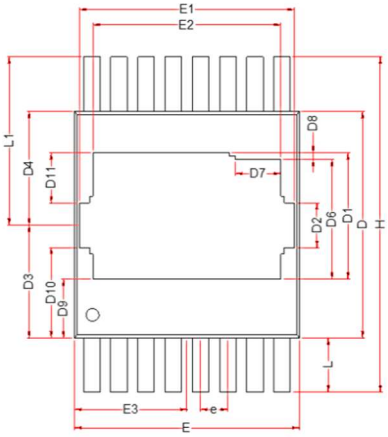
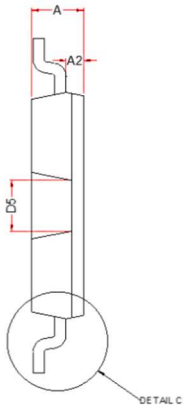
Figure 11 Typ. output charge	Figure 12 Typ. C_{oss} stored energy
	
Q_{OSS} = f(V_{DS}); Freq. = 1 MHz	E_{OSS} = f(V_{DS}); Freq. = 1 MHz

Figure 13 Gate threshold voltage	Figure 14 Drain-source on-state resistance
	
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 10 mA	$R_{DS(on)} = f(T_j)$; I_D = 20 A; V_{GS} = 6 V

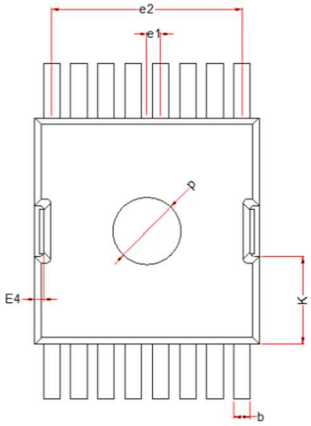
5 Package outlines



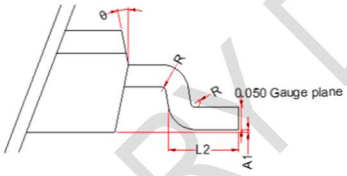
TOP VIEW



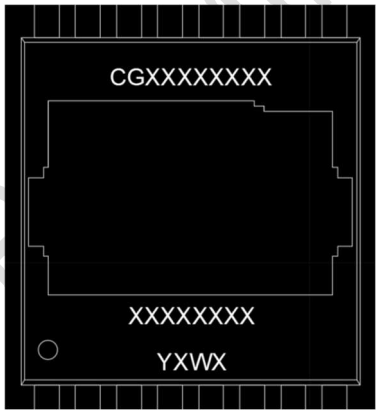
SIDE VIEW



BOTTOM VIEW



DETAIL C



Row	Description	Example
Row 1	Device name	CGXXXXXXXX
Row 2	ASSY lot No.	XXXXXXXX
Row 3	Year & Week	YXWX

Symbol	MIN	MID	MAX
A	2.200	2.275	2.350
A1	0.010	0.060	0.110
A2	0.560	0.760	0.960
b	0.600	0.725	0.850
b1	0.600	0.700	0.800
c	0.450	0.550	0.650
c1	0.450	0.525	0.600
D	10.000	10.150	10.300
D1	5.470	5.670	5.870
D2	1.800	2.000	2.200
D3	4.850	5.050	5.250
D4	5.000	5.065	5.130
D5	2.080	2.280	2.480
D6	5.170	5.370	5.570
D7	1.800	2.000	2.200
D8	0.100	0.300	0.500
D9	2.420	2.620	2.820
D10	3.850	4.050	4.250
D11	2.040	2.240	2.440
E	9.700	9.900	10.100
E1	9.260	9.460	9.660
E2	8.100	8.300	8.500
E3	4.750	4.950	5.150
E4	0.200	0.400	0.600
e		1.200 BSC.	
e1		0.600 BSC.	
e2		8.400 BSC.	
H	14.800	15.000	15.200
K	3.710	3.910	4.110
L	2.250	2.450	2.650
L1	7.300	7.500	7.700
L2	1.300	1.500	1.700
R	0.070	-	-
P	2.900	3.000	3.100
θ	4°	7°	10°

6 Tape and reel information

TBD

7 Revision history

Major changes since the last revision.

Revision	Date	Description of changes
0.8	2024-04-16	0.8 version release