CGK65090TBD

Description

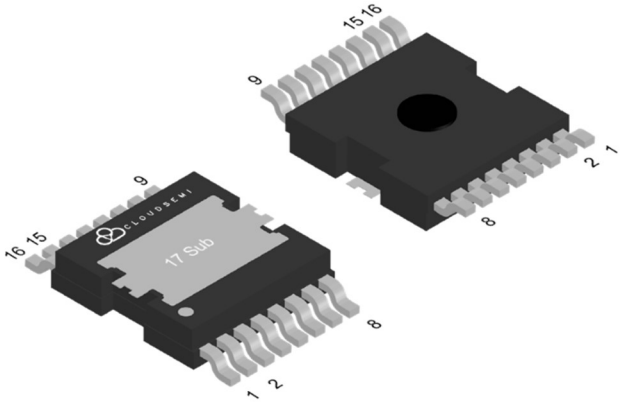
CGK65090TBD is a 650V GaN-on-Si Monolithic Bi-directional Switch (MBDS) in TO-Leaded top-side cooling (TOLT) package. The substrate control IC is monolithically integrated inside the chip. During the four-quadrant switching process of the bidirectional device, the substrate control IC switches the substrate voltage to the low-voltage side to stabilize the dynamic characteristics of the device.

Applications

- AC-DC converters, DC-AC converters
- Three-level-bridge
- Server (Bi-SW active bridge PFC)
- Micro inverters (Cyclo-converter)
- On board charger (Viena rectifier)
- Motor driver (AC/AC matrix converter)
- AC boost converter

Features

- 650V GaN Monolithic Bi-Directional Switch
- $R_{SS(on),\ max}$ 90mΩ
- Thermal enhanced top-cooled TOLT package
- Recommended gate drive voltage 6V
- Ultra-low FOM
- Ultra-high switching frequency to 2MHz
- Zero reverse recovery loss
- RoHS, Pb-free, REACH-compliant



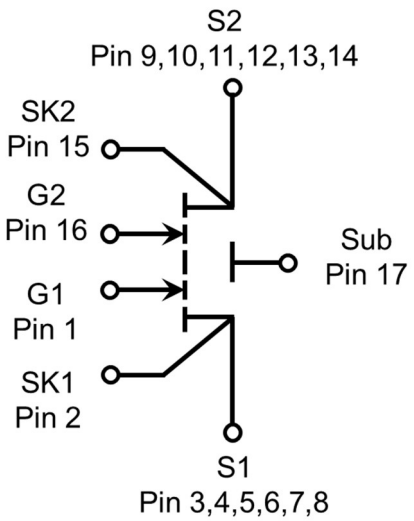


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{SS,\ max}$	650	V
$R_{SS(on),\ max}$	90	mΩ
Q_G	13	nC
Q_{G1}	11	nC
$I_{SS,\ Pulse}$	50	A
Q_{OSS} @ 400 V	80	nC
Q_{OSS1} @ 400 V	65	nC
Q_{rr}	0	nC

Table 2 Ordering Information

Ordering Code	Package	Marking	Packing
CGK65090TBD	TOLT	CGK65090TBD	Reel

Table of Contents

1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

Table 3 Maximum ratings

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-source voltage	$V_{SS, max}$	-	-	650	V	V_{GS} = 0 V; I_{SSS} = 10 μA
Source-source voltage transient [1]	$V_{SS, transient}$	-	-	850	V	V_{GS} = 0 V; V_{SS} = 850V
Continuous current, source-source	I_{SS}	-	-	20	A	T_c = 25 °C; V_{GS} = 6 V
Pulsed current, source-source [2]	$I_{SS, pulse}$	-	-	50	A	
Pulsed current, source-source [2]	$I_{SS, pulse}$	-	-	15	A	T_c = 150 °C; V_{GS} = 6 V
Gate-source voltage, continuous	V_{GS}	-10	-	+7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20	-	+10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open G1 S1 or G2 S2
Power dissipation	P_{tot}	-	-		W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{SS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.
2. Pulse width = 10 μs.

2 Thermal characteristics

Table 4 Thermal characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-		°C/W	
Thermal resistance, junction-ambient	R_{thJA}	-	-		°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

3 Electrical characteristics

at T_j = 25 °C, unless otherwise specified.

Table 5 Static characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{G1S1(TH)}$	1.1	1.7	2.6	V	V_{G2S2} = 6V; V_{S2S1} = 4 mV; I_{S2S1} = 1 mA; T_j = 25 °C
		-	1.9	-		V_{G2S2} = 6V; V_{S2S1} = 4 mV; I_{S2S1} = 1 mA; T_j = 150 °C
	$V_{G2S2(TH)}$	1.1	1.7	2.6	V	V_{G1S1} = 6V; V_{S1S2} = 4 mV; I_{S1S2} = 1 mA; T_j = 25 °C
		-	1.9	-		V_{G1S1} = 6V; V_{S1S2} = 4 mV; I_{S1S2} = 1 mA; T_j = 150 °C
Source-source leakage current	I_{S2S1S}	-	2		μA	V_{G1S1} = 0 V; V_{G2} = V_{S2} = 650 V; T_j = 25 °C
		-	100	-		V_{G1S1} = 0 V; V_{G2} = V_{S2} = 650 V; T_j = 150 °C
	I_{S1S2S}	-	2		μA	V_{G2S2} = 0 V; V_{G1} = V_{S1} = 650 V; T_j = 25 °C
		-	100	-		V_{G2S2} = 0 V; V_{G1} = V_{S1} = 650 V; T_j = 150 °C
Gate-source leakage current	I_{G2S2S}	-	100	-	μA	V_{G2S2} = 6 V; V_{G1S1} = 0 V
	I_{G1S1S}	-	100	-	μA	V_{G1S1} = 6 V; V_{G2S2} = 0 V
Source-source on-state resistance	$R_{S2S1(on)}$	-	60	90	mΩ	V_{G1S1} = 6 V; V_{G2S2} = 6 V; I_{S2} = 20 A; T_j = 25 °C
		-	140	-	mΩ	V_{G1S1} = 6 V; V_{G2S2} = 6 V; I_{S2} = 20 A; T_j = 150 °C
	$R_{S1S2(on)}$	-	60	90	mΩ	V_{G1S1} = 6 V; V_{G2S2} = 6 V; I_{S1} = 20 A; T_j = 25 °C
		-	140	-	mΩ	V_{G1S1} = 6 V; V_{G2S2} = 6 V; I_{S1} = 20 A; T_j = 150 °C
Gate resistance	R_G	-		-	Ω	f = 5 MHz; open G1 S1 or G2 S2

Table 6 CV characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	273	-	pF	V_{G1S1} = 0 V; V_{G2S2} = 6 V; V_{S2S1} = 400 V; f = 1 MHz or V_{G2S2} = 0 V; V_{G1S1} = 6 V; V_{S1S2} = 400 V; f = 1 MHz
Output capacitance	C_{oss}	-	127	-	pF	
Reverse transfer capacitance	C_{rss}	-	11.5	-	pF	
Output charge	Q_{OSS}	-	80	-	nC	
Output Capacitance Stored Energy	E_{OSS}	-	12.5	-	μJ	
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	155	-	pF	V_{G1S1} = 0 V; V_{G2S2} = 6 V; V_{S2S1} = 400 V or V_{G2S2} = 0 V; V_{G1S1} = 6 V; V_{S1S2} = 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	198	-	pF	
Input capacitance	C_{iss1}	-	272	-	pF	V_{G1S1} = 0 V; V_{G2} = V_{S2} = 400 V; f = 1 MHz or V_{G2S2} = 0 V; V_{G1} = V_{S1} = 400 V; f = 1 MHz
Output capacitance	C_{oss1}	-	127	-	pF	
Reverse transfer capacitance	C_{rss1}	-	11.3	-	pF	
Output charge	Q_{OSS1}	-	65	-	nC	
Output Capacitance Stored Energy	E_{OSS1}	-	11.5	-	μJ	
Effective output capacitance, energy related [1]	$C_{o(er)1}$	-	143	-	pF	V_{G1S1} = 0 V; V_{G2S2} = 6 V; V_{S2S1} = 400 V or V_{G2S2} = 0 V; V_{G1S1} = 6 V; V_{S1S2} = 400 V
Effective output capacitance, time related [2]	$C_{o(tr)1}$	-	161	-	pF	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{SS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{SS} is rising from 0 to 400 V.

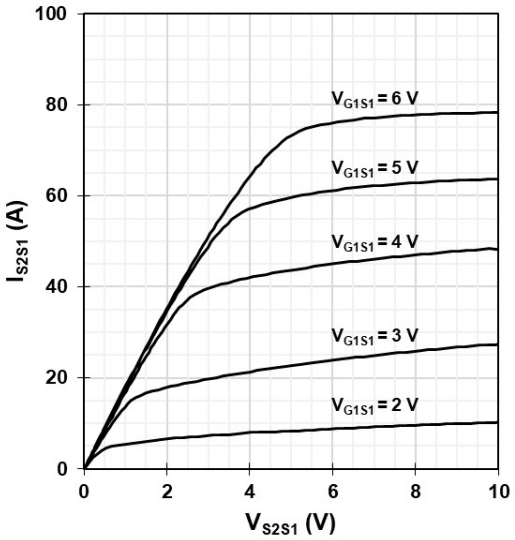
Table 7 Gate charge characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	13	-	nC	V_{G1S1} = 0 to 6 V; V_{G2S2} = 6 V; V_{S2S1} = 400 V; I_{S2S1} = 20 A or V_{G2S2} = 0 to 6 V; V_{G1S1} = 6 V; V_{S1S2} = 400 V; I_{S1S2} = 20 A
Gate-source charge	Q_{GS}	-	2.2	-	nC	
Gate charge	Q_{G1}	-	11	-	nC	V_{G1S1} = 0 to 6 V; V_{G2} = V_{S2} = 400 V; I_{S2S1} = 20 A or V_{G2S2} = 0 to 6 V; V_{G1} = V_{S1} = 400 V; I_{S1S2} = 20 A
Gate-source charge	Q_{GS1}	-	2	-	nC	

4 Electrical characteristics diagrams

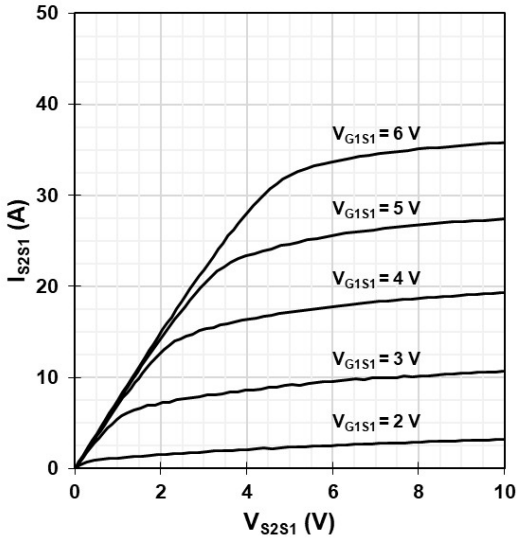
at T_j = 25 ºC, unless otherwise specified.

Figure 1 Typ. output characteristics



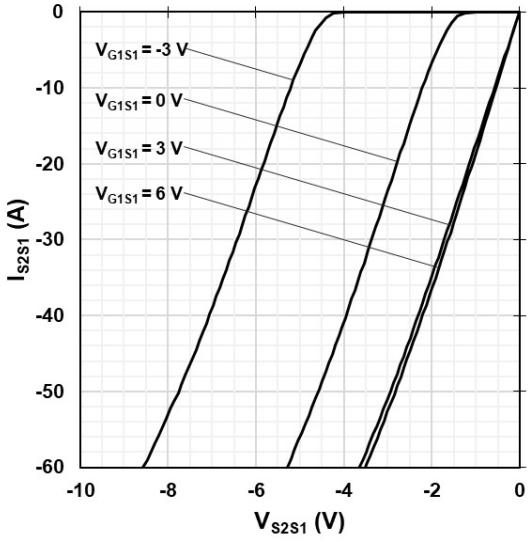
$I_{S2S1} = f(V_{S2S1}, V_{G1S1})$; V_{G2S2} = 6V; T_j = 25 ºC

Figure 2 Typ. output characteristics



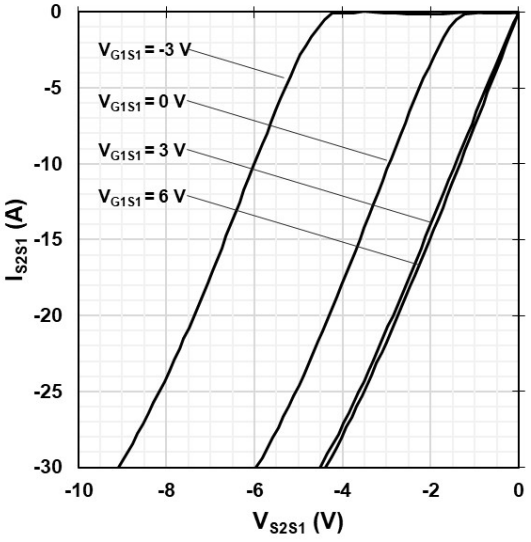
$I_{S2S1} = f(V_{S2S1}, V_{G1S1})$; V_{G2S2} = 6V; T_j = 150 ºC

Figure 3 Typ. third quadrant conduction



$I_{S2S1} = f(V_{S2S1}, V_{G1S1})$; V_{G2S2} = 6V; T_j = 25 ºC

Figure 4 Typ. third quadrant conduction



$I_{S2S1} = f(V_{S2S1}, V_{G1S1})$; V_{G2S2} = 6V; T_j = 150 ºC

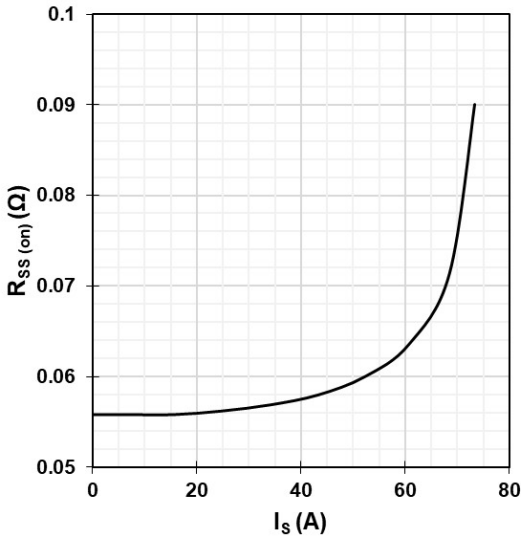
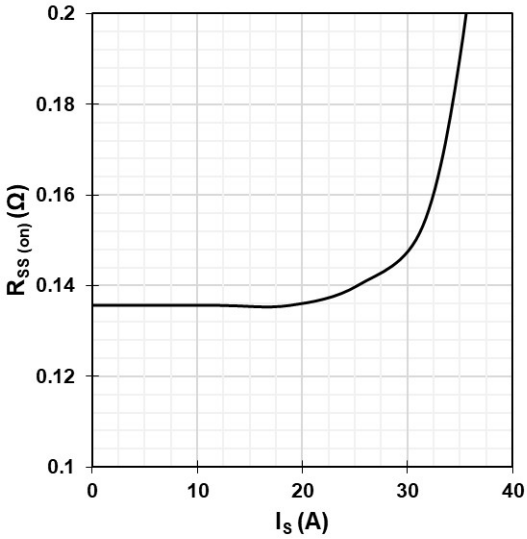
Figure 5 Typ. on-state resistance	Figure 6 Typ. on-state resistance
	
$R_{SS(on)} = f(I_S, V_{GS})$; V_{G1S1} = 6V; V_{G2S2} = 6V; T_j = 25 °C	$R_{SS(on)} = f(I_S, V_{GS})$; V_{G1S1} = 6V; V_{G2S2} = 6V; T_j = 150 °C

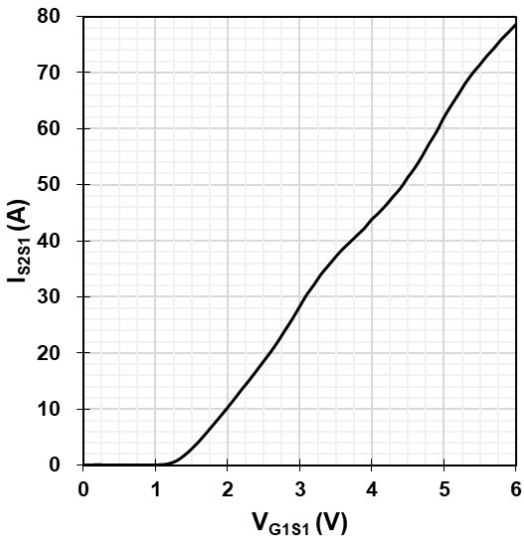
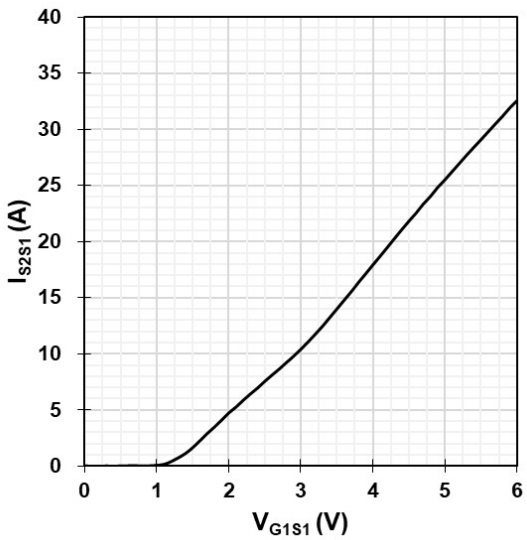
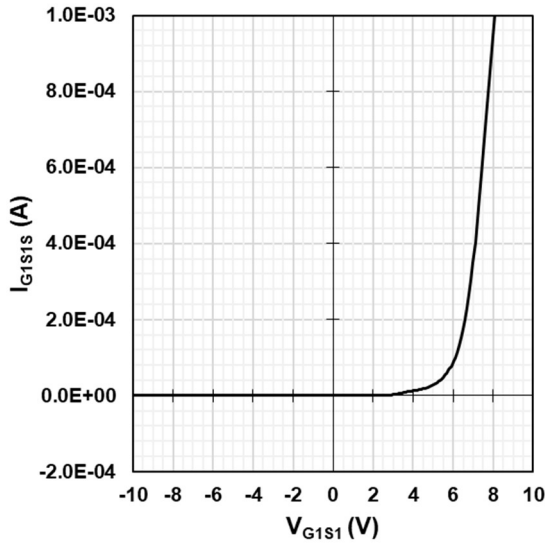
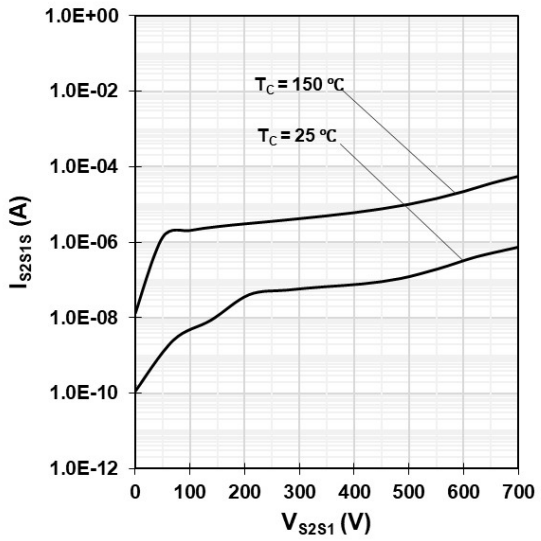
Figure 7 Typ. transfer characteristics	Figure 8 Typ. transfer characteristics
	
$I_{S2S1} = f(V_{G1S1})$; V_{S2S1} = 5 V; V_{G2S2} = 6 V; T_j = 25 °C	$I_{S2S1} = f(V_{G1S1})$; V_{S2S1} = 5 V; V_{G2S2} = 6 V; T_j = 150 °C

Figure 9 Typ. gate-to-source leakage



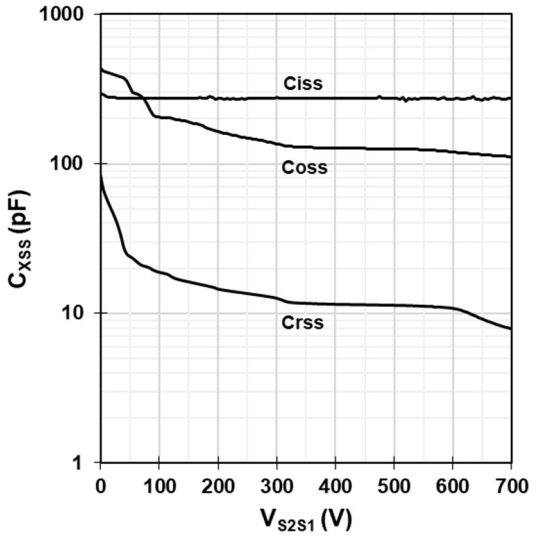
$I_{G1S1S} = f(V_{G1S2})$; $V_{G2} = V_{S2}$ = open

Figure 10 Typ. source-to-source leakage



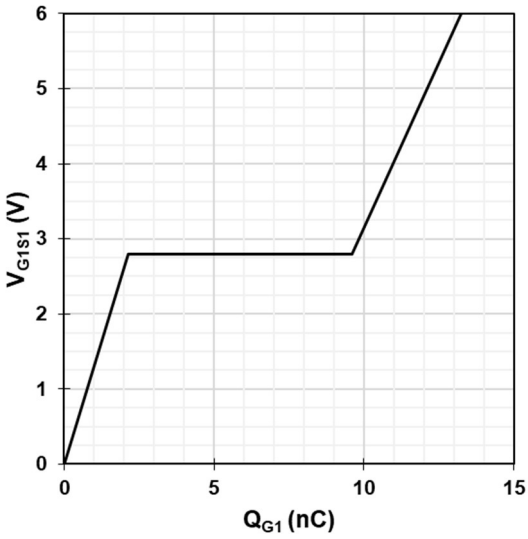
$I_{S2S1S} = f(V_{S2S1})$; $V_{G1S1} = 0V$; $V_{G2S2} = 0V$

Figure 11 Typ. capacitances



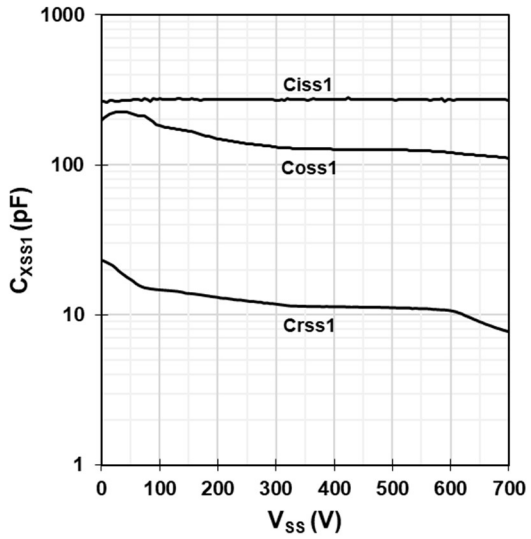
$C_{XSS} = f(V_{S2S1})$; $V_{G1S1} = 0V$; $V_{G2S2} = 6V$; Freq. = 1 MHz

Figure 12 Typ. gate charge



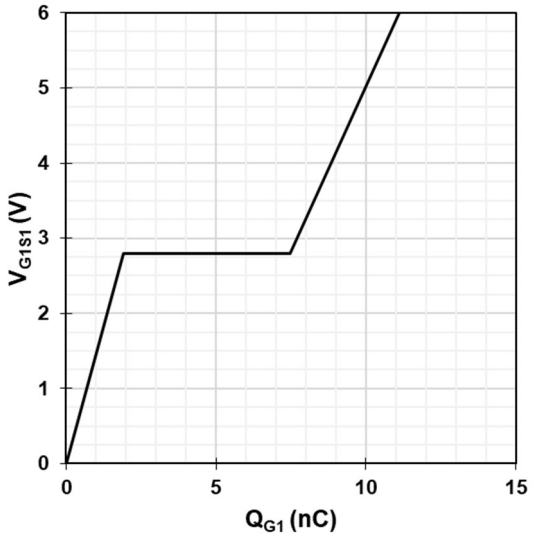
$V_{G1S1} = f(Q_{G1})$; $V_{G2S2} = 6V$

Figure 13 Typ. capacitances



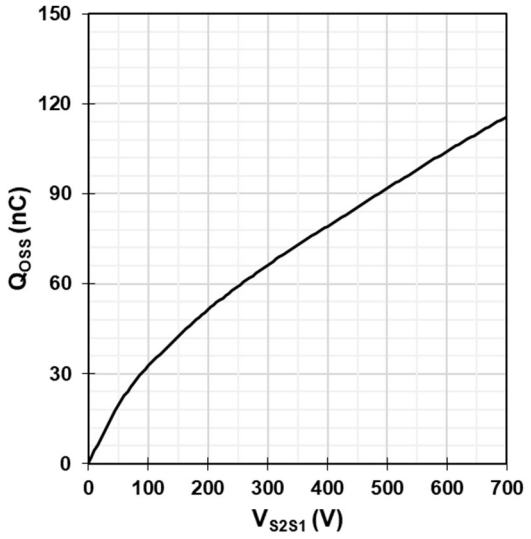
C_{XSS1} = f(V_{SS}); V_{GS} = 0V; Freq. = 1 MHz

Figure 14 Typ. gate charge



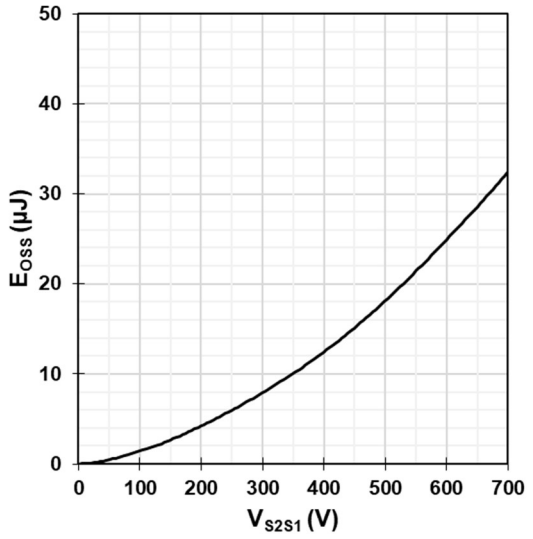
V_{G1S1} = f(Q_{G1}); V_{G2S2} = 0V

Figure 15 Typ. output charge



Q_{OSS} = f(V_{S2S1}); V_{G1S1} = 0V; V_{G2S2} = 6V Freq. = 1 MHz

Figure 16 Typ. C_{oss} stored energy



E_{OSS} = f(V_{S2S1}); V_{G1S1} = 0V; V_{G2S2} = 6V Freq. = 1 MHz

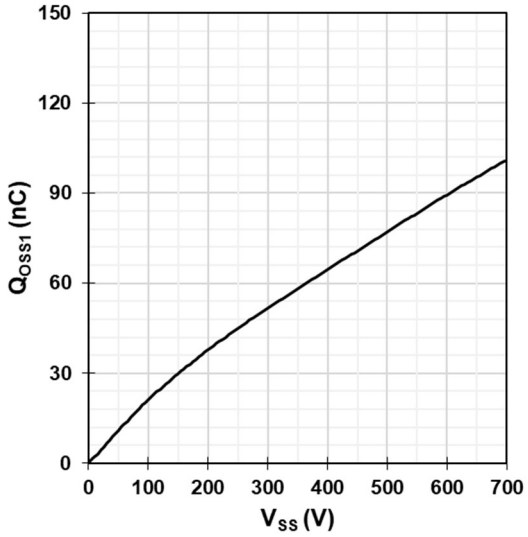
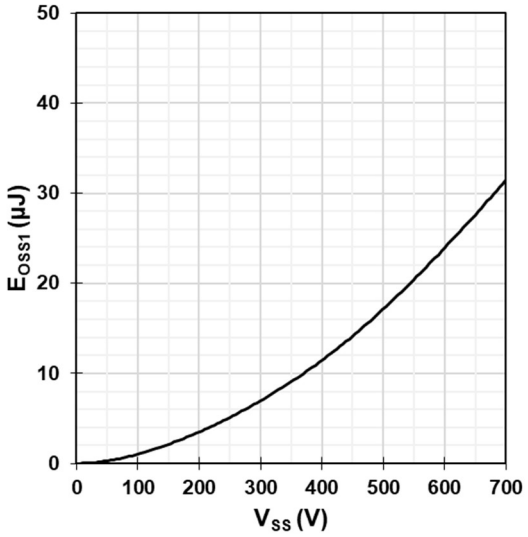
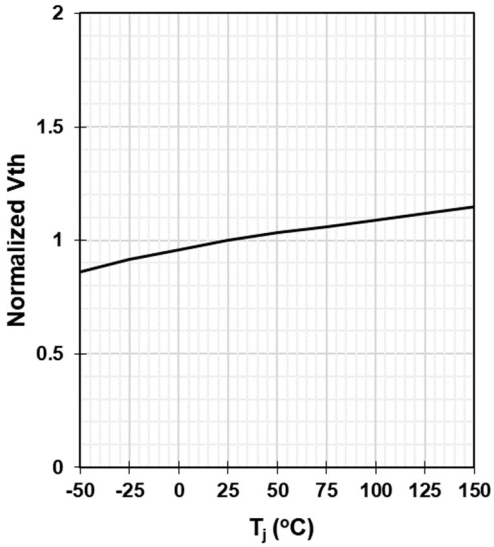
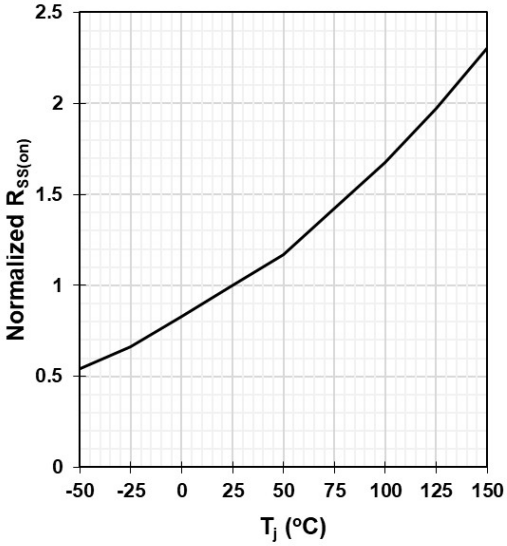
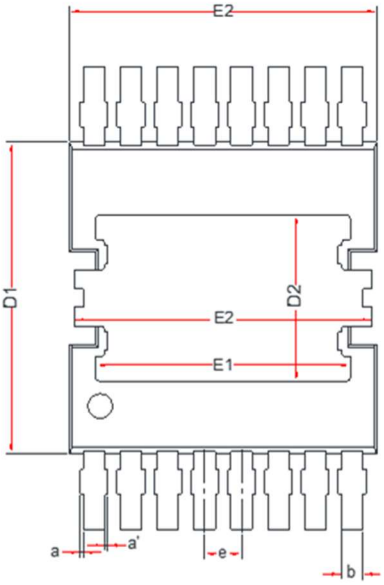
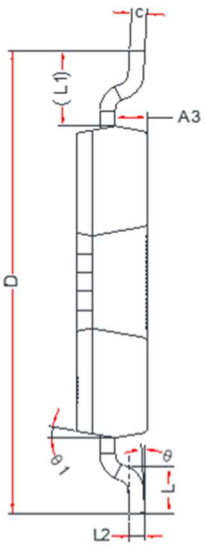
Figure 17 Typ. output charge	Figure 18 Typ. C_{oss} stored energy
	
Q_{OSS1} = f(V_{SS}); V_{GS} = 0V; Freq. = 1 MHz	E_{OSS1} = f(V_{SS}); V_{GS} = 0V; Freq. = 1 MHz

Figure 19 Gate threshold voltage	Figure 20 Source-source on-state resistance
	
$V_{G1S1(TH)}$ = f(T_j); V_{G2S2} = 6V; V_{S2S1} = 4 mV; I_{S2} = 1 mA	$R_{SS(on)}$ = f(T_j); V_{G1S1} = 6 V; V_{G2S2} = 6 V; I_{S2} = 20 A

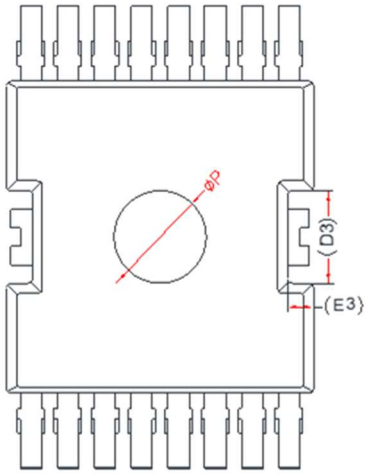
5 Package outlines



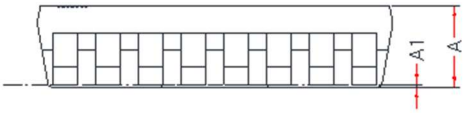
TOP VIEW



SIDE VIEW

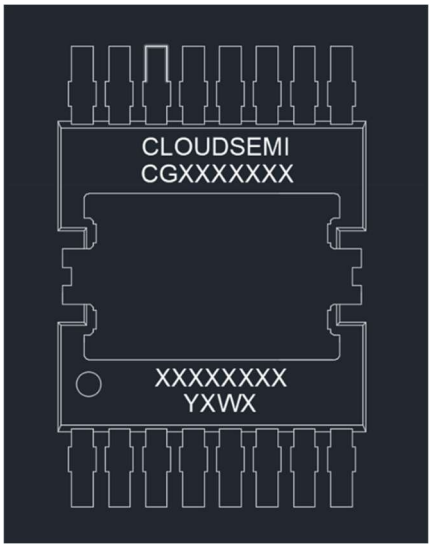


BOTTOM VIEW



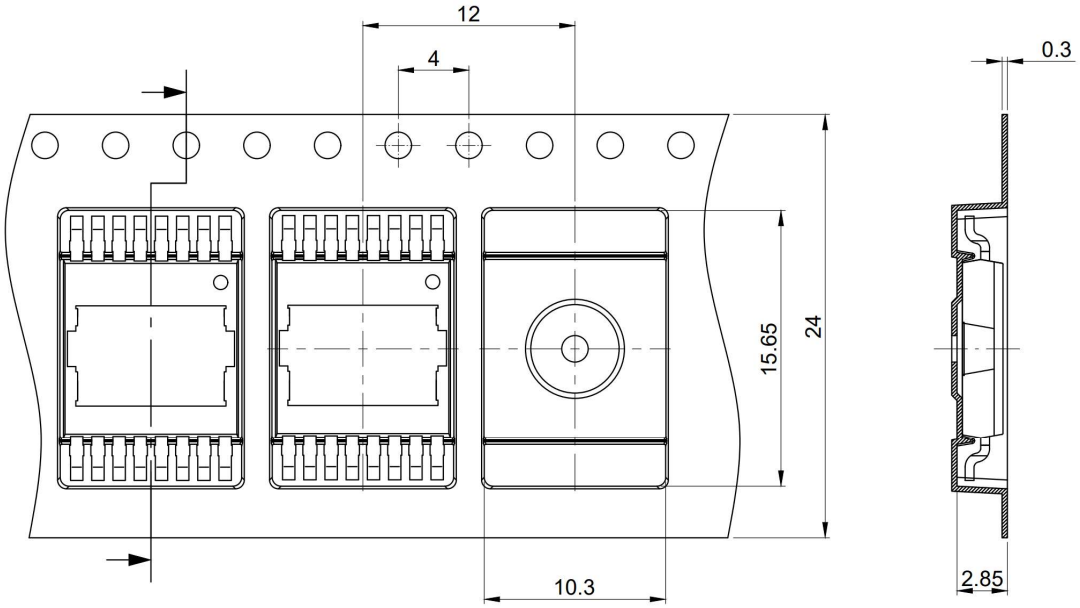
SIDE VIEW

Row	Description	Example
Row1	Company Logo	CLOUDSEMI
Row2	Device name	CGXXXXXXXX
Row3	ASSY lot No.	XXXXXXXX
Row4	Year & Week	YXWX



Symbol	MIN	MID	MAX
A	2.25	2.30	2.35
A1	0.01	0.08	0.16
A3	0.99	1.04	1.09
a	0.00	-	0.15
a'	0.00	-	0.15
b	0.60	0.70	0.80
c	0.40	0.50	0.60
D	14.80	15.00	15.20
D1	10.00	10.10	10.30
D2	5.30	5.40	5.50
D3		3.00REF	
E	9.70	10.00	10.10
E1	8.20	8.30	8.40
E2	9.50	9.70	9.90
E3		0.85REF	
e	1.10	1.20	1.30
L	1.40	1.50	1.60
L1		2.45REF	
L2		0.50BSC	
ØP	2.90	3.00	3.10
θ	0°	-	8°
θ1	8°	10°	12°

6 Tape information



All dimensions are in units mm

7 Revision history

Major changes since the last revision.

Revision	Date	Description of changes
0.1	2025-09-03	0.8 version release