CG65055D0-CP

Description

CG65055D0-CP is 650V GaN-on-Si enhancement-mode power transistor bare wafer manufactured on CloudSemi 6-inch platform. The CG65055D0-CP features dual gate pads for optimal module layout and parallel method. The properties of GaN allow for high current, high breakdown voltage and high switching frequency.

Features

- 650V GaN enhancement-mode power switch
- $R_{DS(on),\ max}$ 55mΩ
- Recommended gate drive voltage 0V ~ 6V
- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss
- Monolithic integrated ESD protection, HBM class 2, CDM class C3

Applications

- AC-DC converters, DC-DC converters
- Bridgeless totem pole PFC, data center, telecom, network SMPS
- Uninterruptable power supplies (UPS)
- Solar inverters, energy storage systems
- Wireless power transfer
- Power adapters, LED lighting drivers
- Laser drivers
- Industrial motor drives

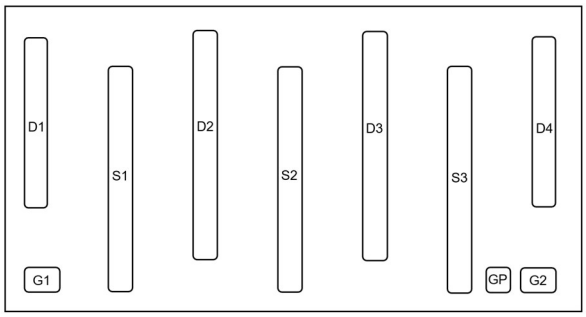
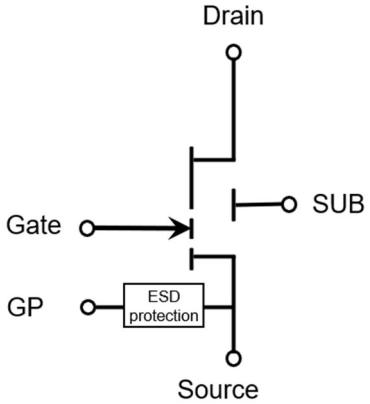


Table 1 Key Performance Parameters at T_j = 25 °C

Parameters	Values	Units
$V_{DS,\ max}$	650	V
$R_{DS(on),\ max}$ [1]	55	mΩ
$Q_{G,\ typ}$	6.3	nC
$I_{D,\ Pulse}$ [2]	70	A
Q_{OSS} @ 400 V	60	nC
Die size	4.6836 x 2.4728	mm^2
Wafer thickness	1000	μm



1. Defined by chip design. Die is not tested to full current in production.
2. Performance will vary based on assembly technique and substrate of choice.

Table 2 Ordering Information

Part number	Ordering Code	Packing
CG65055D0-CP	CG65055D0-CP	Contact CloudSemi

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1 Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

Table 3 Maximum ratings

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	650	V	V_{GS} = 0 V; I_D = 10 μA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	850	V	V_{GS} = 0 V; V_{DS} = 850 V
Continuous current, drain-source	I_D	-	-	35	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	70	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	30	A	T_c = 150 °C; V_G = 6 V
Gate-source voltage, continuous [3]	V_{GS}	-7	-	+7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-20	-	+10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns; f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	169	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.
2. Performance will vary based on assembly technique and substrate of choice.
3. Pulse width = 10 μs. Performance will vary based on assembly technique and substrate of choice.
4. The minimum V_{GS} is clamped by ESD protection circuit.

2 Electrical characteristics

at T_j = 25 °C, unless otherwise specified.

Table 4 Static characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.1	1.7	2.6	V	I_D = 8 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.9	-		I_D = 8 mA; V_{DS} = V_{GS}; T_j = 150 °C
Drain-source leakage current	I_{DSS}	-	1	20	μA	V_{DS} = 650 V; V_{GS} = 0 V; T_j = 25 °C
		-	25	-		V_{DS} = 650 V; V_{GS} = 0 V; T_j = 150 °C
Gate-source leakage current	I_{GSS}	-	50	-	μA	V_{GS} = 6 V; V_{DS} = 0 V
Reverse Gate leakage current	I_{RGL}		-15		nA	V_{GS} = -6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	42	55	mΩ	V_{GS} = 6 V; I_D = 10 A; T_j = 25 °C
		-	105	-	mΩ	V_{GS} = 6 V; I_D = 10 A; T_j = 150 °C
Gate resistance	R_G	-	1.6	-	Ω	f = 5 MHz; open drain

1. Defined by chip design. Die is not tested to full current in production.

Table 5 Dynamic characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	227	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Output capacitance	C_{oss}	-	60	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Reverse transfer capacitance	C_{rss}	-	0.8	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	102	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	151	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	60	-	nC	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Output Capacitance Stored Energy	E_{OSS}	-	8.2	-	μJ	
Turn-on delay time	$t_{d(on)}$	-	8.5	-	ns	V_{DS} = 400 V; I_D = 15 A; L = 90 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 1 Ω
Turn-off delay time	$t_{d(off)}$	-	10.7	-	ns	
Rise time	t_r	-	6.4	-	ns	
Fall time	t_f	-	5.9	-	ns	
Switching Energy during turn-on	E_{on}	-	48	-	μJ	
Switching Energy during turn-off	E_{off}	-	7.8	-	μJ	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 6 Gate charge characteristics

Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	6.3	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 35 A
Gate-source charge	Q_{GS}	-	1.6	-	nC	
Gate-drain charge	Q_{GD}	-	1.9	-	nC	
Gate plateau voltage	V_{plat}	-	2.9	-	V	V_{DS} = 400 V; I_D = 35 A

Table 7 Reverse conduction characteristics

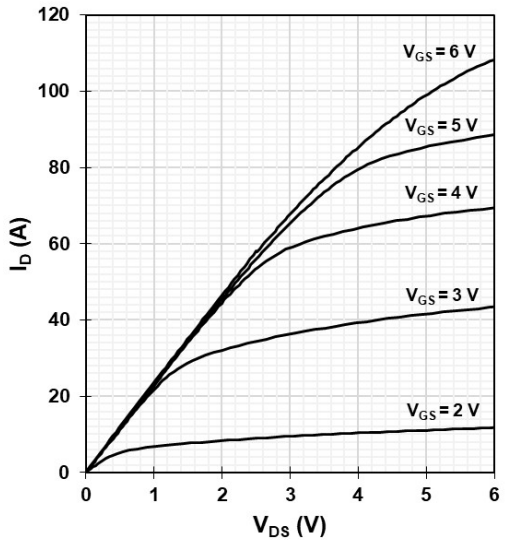
Parameters	Sym.	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	3.8	-	V	V_{GS} = 0 V; I_{SD} = 35 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	60	-	A	V_{GS} = 6 V
Reverse recovery charge [1]	Q_{rr}	-	0	-	nC	I_{SD} = 35 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{OSS}

3 Electrical characteristics diagrams

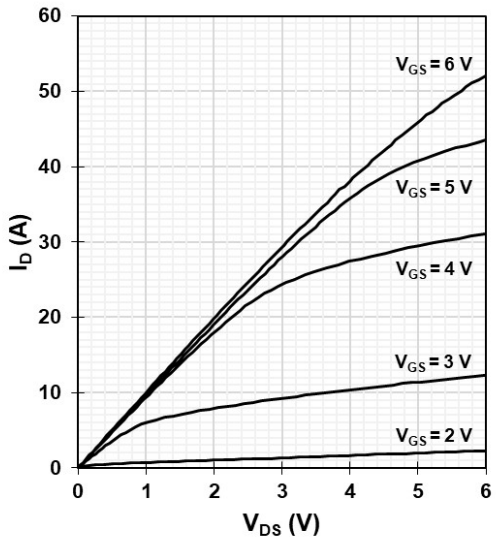
at T_j = 25 °C, unless otherwise specified.

Figure 1 Typ. output characteristics



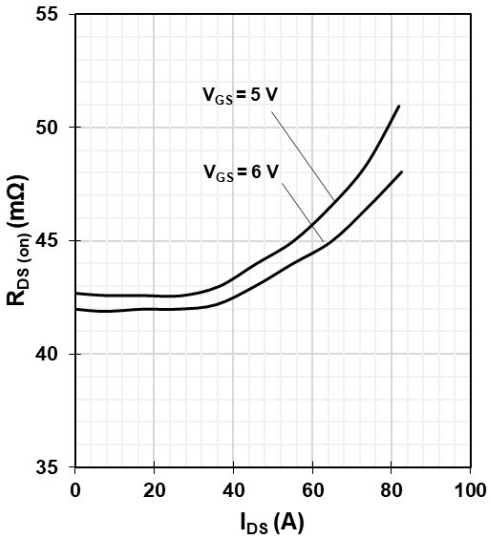
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



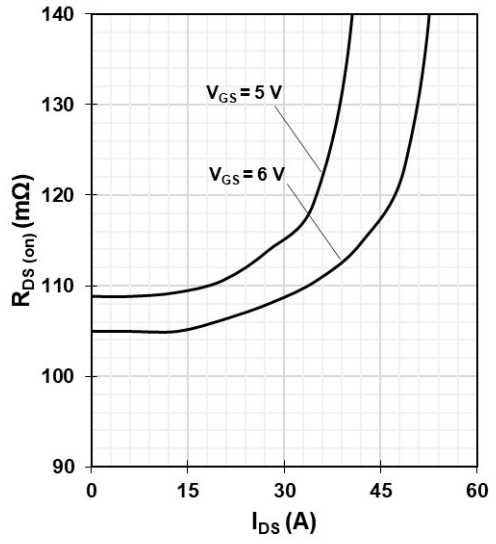
$I_D = f(V_{DS}, V_{GS})$; T_j = 150 °C

Figure 3 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 150 °C

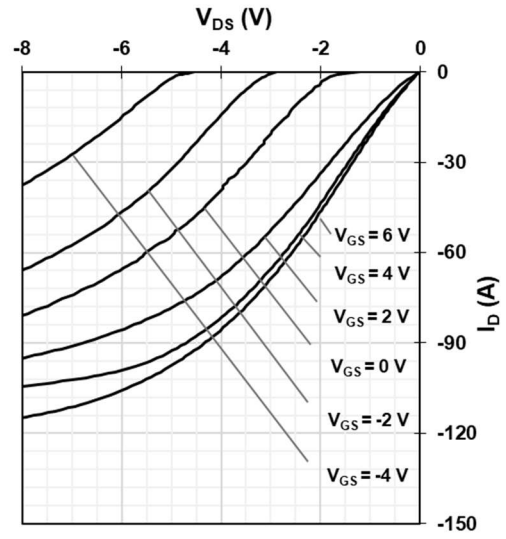
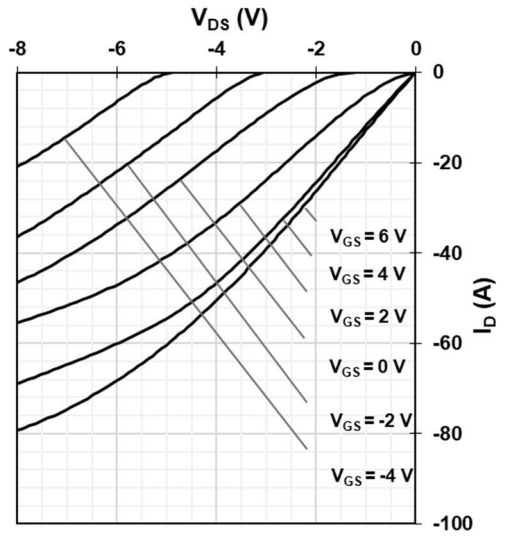
Figure 5 Typ. channel reverse characteristics	Figure 6 Typ. channel reverse characteristics
	
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C	$I_D = f(V_{DS}, V_{GS})$; T_j = 150 °C

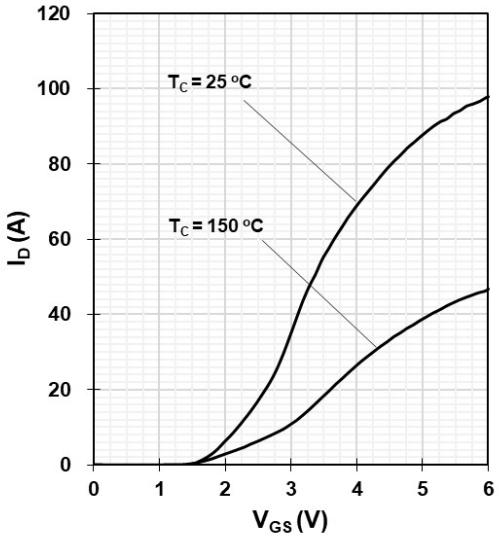
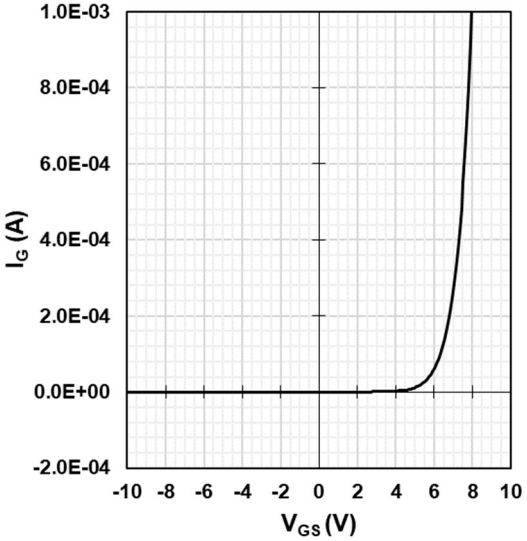
Figure 7 Typ. transfer characteristics	Figure 8 Typ. gate-to-source leakage
	
$I_D = f(V_{GS})$; V_{DS} = 5 V	$I_G = f(V_{GS})$; V_D = open

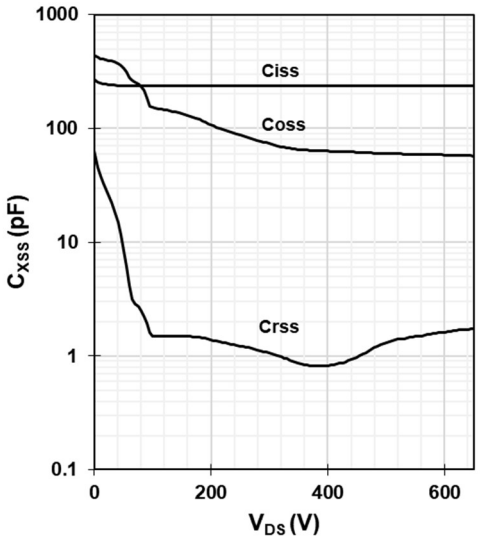
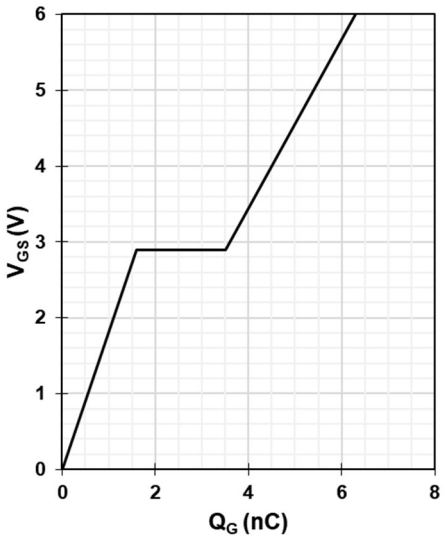
Figure 9 Typ. capacitances	Figure 10 Typ. gate charge
	
C_{XSS} = f(V_{DS}); Freq. = 1 MHz	V_{GS} = f(Q_G); V_{DS} = 400 V; I_D = 30 A

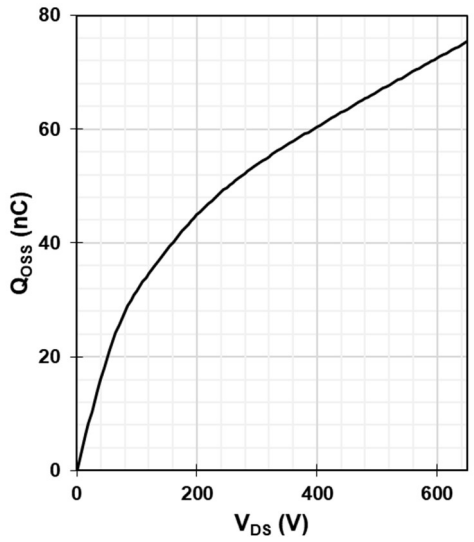
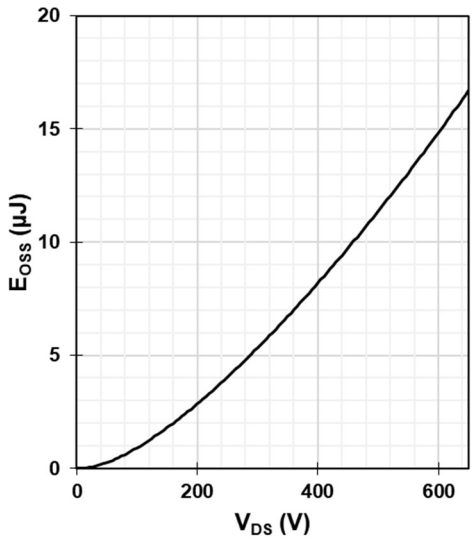
Figure 11 Typ. output charge	Figure 12 Typ. C_{oss} stored energy
	
Q_{OSS} = f(V_{DS}); Freq. = 1 MHz	E_{OSS} = f(V_{DS}); Freq. = 1 MHz

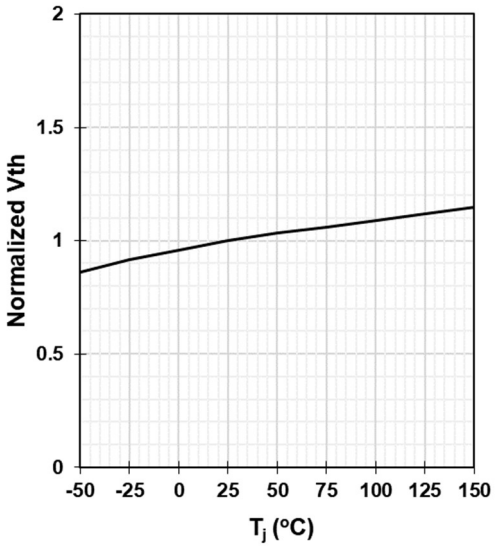
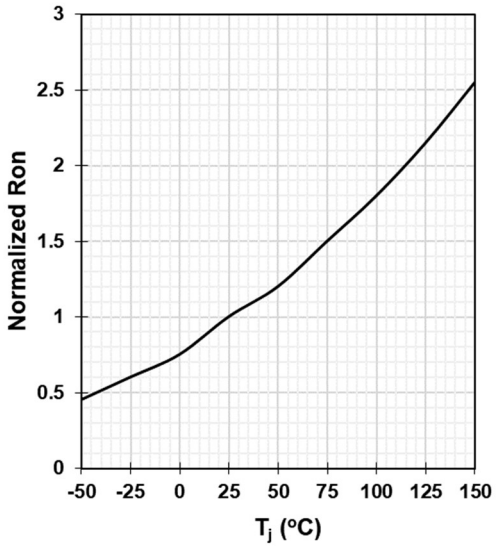
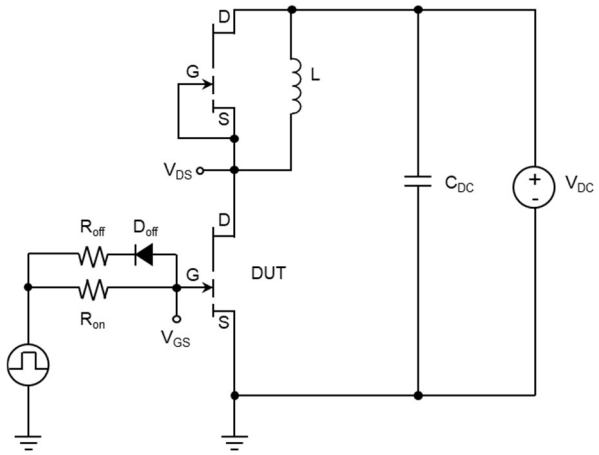
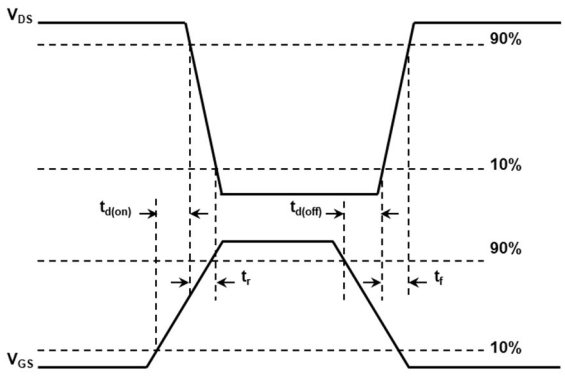
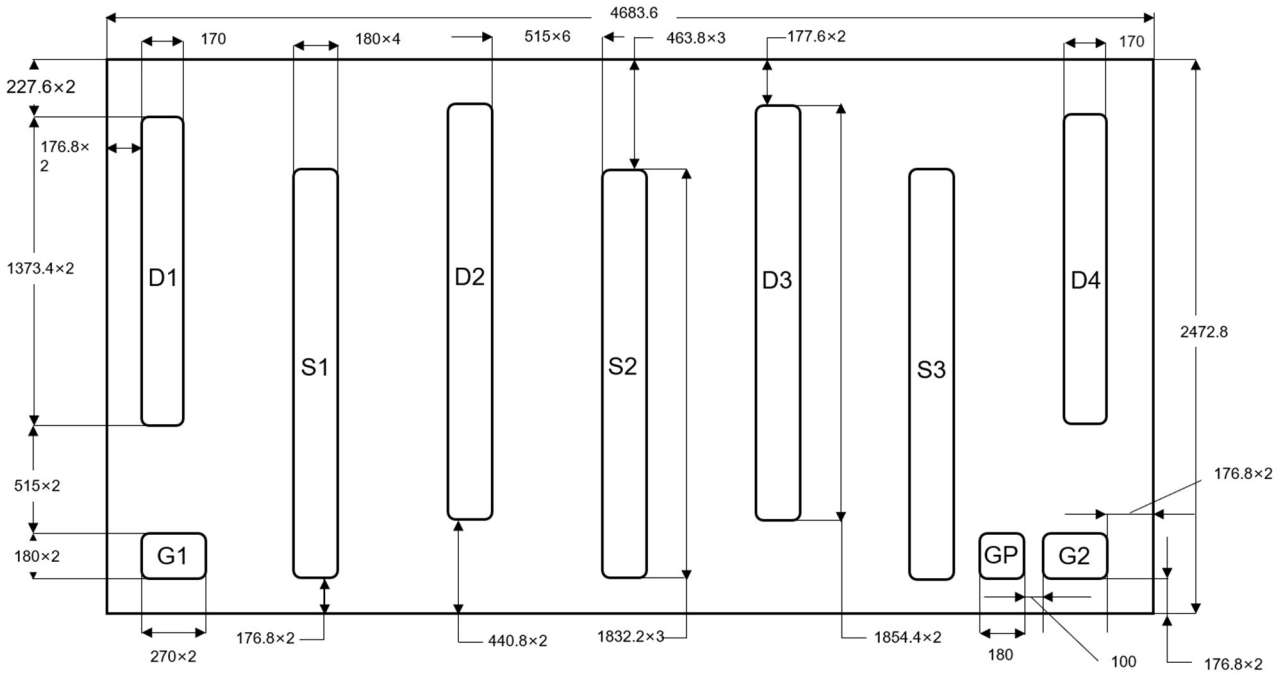
Figure 13 Gate threshold voltage	Figure 14 Drain-source on-state resistance
	
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; I_D = 8 mA	$R_{DS(on)} = f(T_j)$; I_D = 10 A; V_{GS} = 6 V

Figure 15 Switching time test circuit	Figure 16 Typ. switching time waveform
	
V_{DS} = 400 V, I_D = 15 A, L = 90 μH, V_{GS} = 6 V, R_{on} = 10 Ω, R_{off} = 1 Ω	

4 Dimensions

There are 10 dedicated bonding pad areas, 3 for the Source, 4 for the Drain, 2 for the Gate and 1 for the GP.



Wafer features	Values	Units
Wafer size	6	inch
Wafer thickness	1000	μm
Gross die per wafer	1210	
Die size (with scribe line)	4.6836 x 2.4728	mm^2
Scribe line width	80	μm
Top metallization	Al-Cu	
Top metal thickness	4.5	μm
Top passivation	SiO_2 / SiN / Polyimide	
Gate pad size	270 x 180	$μm^2$
GP pad size [1]	180 x 180	$μm^2$
Source pad size	180 x 1832.3	$μm^2$
Drain pad size	D1, D4:170 x 1373.4 D2, D3:180 x 1854.4	$μm^2$
Backside	Silicon	

1. The GP pad is ESD protection IC port and should be electrically connected to the Gate through package.
2. All the pad size refers to top passivation opening size.

5 Revision history

Major changes since the last revision.

Revision	Date	Description of changes
1.0	2024-08-21	1.0 version release